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Performance Analysis of Three Level Inverter for L & LCL Filters Connected To Grid

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Abstract— Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. In multi level inverters the most important topologies like diode-clamped inverters (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multi cell with separate dc sources. Diode-clamped inverter results in the low frequency voltage ripple in the NP, which is the point between the two dc-link capacitors. This explores the fundamental limitations of the NP voltage balancing problem for different loading conditions of three-level voltage source converters. It also represents that the most relevant control and modulation methods developed for the space-vector modulation technique. Design of L and LCL filter is done for three level diode clamped inverter connected to grid. Three phase VSI are switched by these PWM pulses to improve the output waveforms of the three level diode clamped inverter connected to grid using filters. The procedure for designing an LCL-filter is proposed and verified by simulations. This paper proposed method PWM waveforms are generated by SVPWM technique using MATLAB/SIMULINK and L and LCL filter is designed connected to grid.

Keywords— *Diode-clamped inverter, multilevel inverter, Space vector PWM, Three-level inverter, L & LCL filters.*

1 INTRODUCTION

The area of multilevel power conversion can still be considered young. In 1980, early interest in multilevel power conversion technology was triggered by the work of Nabae, etal., who introduced the neutral-point-clamped (NPC) inverter topology. It was immediately realized that this new converter had many advantages over the more conventional two-level inverter. Subsequently, in the early nineties the concept of the three-level converter was extended further and some new multilevel topologies were proposed. At the present time, the majority of research and development effort seems to concentrate on the development of three classes of converters: the diode-clamped multilevel converter, the multilevel converter with cascaded single-phase H-bridge inverters, and the multilevel converter known as the flying capacitor converter, or sometimes as the imbricated cells multilevel converter. As mentioned, the three-level NPC converter was the first widely popular multilevel topology.

The introduction of the NPC converter, the original topology was extended to a higher number of levels using the same principle of diode-clamped intermediate voltage levels.

The concept of space voltage vectors corresponding to various switching states has been applied to study the impact of various switching states on the capacitor charge balancing in almost every paper discussing the SVM approach. An advantage of the SVM is the instantaneous control of switching states and the freedom to select vectors in order to balance the NP. Additionally, one can realize output voltages with almost any average value by using the nearest three vectors, which is the method that results in the best spectral performance. The primary constraint in devising SVM (as is the case with in most multilevel modulation techniques) involves minimizing the harmonic content of the output PWM waveform while at the same time maintaining the capacitor charge balance. With respect to modeling and control of three level converters, the dominant approach is to divide and conquer. The phase legs are treated essentially as voltage sources while the charge balance becomes part of the modulator, which selects between the redundant switching states in order to maintain the charge balance in the split dc-link capacitors.

In this paper Simulink model of a three-level converter that included the NP voltage using SVPWM technique is done and the design of L and LCL filters was developed and connected to grid using MATLAB/Simulink [8] to give pure sinusoidal waveform to grid.

2 THREE LEVEL INVERTER

Switching states that are shown in Fig.1 can represent the operating status of the switches in the three-level NPC inverter. When switching state is '1', it is indicated that upper two switches in leg A connected and the inverter terminal voltage V_{AZ}, which means the voltage for terminal A with respect to the neutral point Z, is +E, whereas '-1' denotes that the lower two switches are on, which means V_{AZ} = -E. When switching state '0', it indicates that the inner two switches S_2 and S_3 are connected and V_{AZ} =0 through the clamping diode, depending on the direction of the load current ia.

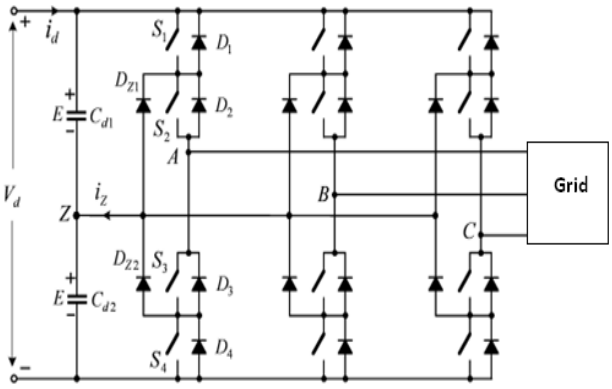

Fig 1: Three-level Neutral Point Clamped inverter [1].

When D_{Z1} is turn on, the load current will be positive and the terminal A will be connected to the neutral point Z through the conduction of D_{Z1} and S_2. Table 1 shows switching status for leg A. Leg B and leg C have the same concept.

Table.1 Definition of Switching States

Switching states	Device switching states(Phase A)				Inverter terminal voltage Vaz
	S1	S2	S3	S4	
1	On	On	Off	Off	E
0	Off	On	On	Off	0
-1	Off	Off	On	On	-E

3 SPACE VECTOR MODULATION

Space vector pulse width modulation (SVM) is quite different from the PWM methods. With PWMs, the inverter can be thought of as three separate push-pull driver stages which create each phase waveform independently. SVM however treats the inverter as a single unit. Specifically the inverter can be driven to eight unique states. Modulation is accomplished by switching the state of inverter. SVM is a digital modulation technique where the objective is to generate PWM load line voltages. This is done in each sampling period by properly selecting the switching states of inverter and calculation of the appropriate time period for each state.

4 STATIONARY SPACE VECTORS

Three switching states [1], [0] and [-1] can represent the operation of each leg. By taking all three phases into account, the inverter has a total of 27 possible switching states. Table 3 shows the possibility of three phase switching states that are represented by three letters in square brackets for the inverter phases A, B, and C. The voltage has four groups.

a. Zero vector (V_1, V_2, V_3), representing three switching states [1 1 1], [-1 -1 -1] and [0 0 0]. The magnitude of V1, V2, and V3 is Zero.
b. Small vector (V_4 to V_{15}), all having a magnitude of $V_d/3$. Each small sector has two switching states, one containing [1] and the other containing [-1] and they classified into P- or N- type small vector.
c. Medium vectors (V_{17}, V_{19}, V_{21}, V_{23}, V_{15}, V_{27}), whose magnitude is $\frac{\sqrt{3}}{3}Vd$.
d. Large vectors (V_{16}, V_{18}, V_{20}, V_{22}, V_{24}, V_{26}), all having a magnitude of $\frac{2}{3}$Vd.

5 TIME CALCULATION

The space vector diagram that is shown in Figure.4 can be used to calculate the time for each sector (I to VI). Each sector has four regions (1 to 4), with the switching states of all vectors.

By using the same strategy that was used in chapter two, the sum of the voltage multiplied by the interval of choose space vector equals the product of the reference voltage *Vref* and sampling period T_s. To illustrate, when reference voltage is located in region 2 of sector I then the nearest vectors to reference voltage areV_5 ,V_{17}, and V_7 as shown in Fig. 2, and the next equations explain the relationship between times and voltages :-

$$V_5 T_a + V_{17} T_b + V_7 T_c = V_{ref} T_s, \quad (1)$$

$$T_a + T_b + T_c = T_s \quad (2)$$

Where Ta, Tb and Tc are the times for V_5, V_{17} and V_7 respectively.

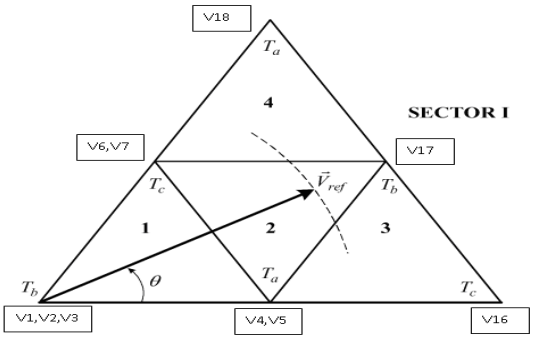

Fig 2: Voltage vector and their times[4].

From Fig. 2 voltage sectors V_5 ,V_7 andV_{17} can be observed as follow:-

$$V_5 = \frac{1}{3}V_d, \quad V_7 = \frac{1}{3}V_d e^{\frac{j\pi}{3}}, V_{17} = \frac{\sqrt{3}}{3}V_d e^{\frac{j\pi}{6}}, \quad V_{ref} = V_{ref} e^{j\theta} \quad (3)$$

By substituting equation (3) into (1), we get

$$\frac{1}{3}V_dT_a + \frac{\sqrt{3}}{3}V_d\left(cos\frac{\pi}{6} + jsin\frac{\pi}{6}\right)T_b + \frac{1}{3}V_d\left(cos\frac{\pi}{3} + jsin\pi 3Tc = Vref(cos\theta + jsin\theta)Ts \quad (4)$$

From equation (4) real part and imaginary part can be determined by following Equations

$$T_a + \frac{3}{2}T_b + \frac{1}{2}T_c = 3\frac{Vref}{Vd}(\cos\theta)T_s \quad (5)$$

$$\frac{3}{2}T_b + \frac{\sqrt{3}}{2}T_c = 3\frac{Vref}{Vd}(\sin\theta)T_s \quad (6)$$

By solving equation (5) & (6) with the equation for total time Ts = Ta + Tb + Tc, for $0 \le \Theta \le \pi/3$.

$$T_a = T_s[1 - 2m_a \sin\theta]$$

$$T_b = T_s\left[2m_a \sin(\frac{\pi}{3} + \theta) - 1\right]$$

$$T_c = T_s\left[1 - 2m_a \sin(\frac{\pi}{3} + \theta)\right] \quad (7)$$

Where *ma* is the modulation index and can be expressed as follow:-

$$m_a = \sqrt{2}\frac{V_{ref}}{V_d} \quad (8)$$

The maximum value for V ref can be derived at medium vector voltage

$$V_{ref,max} = \frac{\sqrt{3}}{3}V_d \quad (9)$$

And the modulation index can be given as below

$$0 \le m_a \le 1$$

The equations for the calculation of times for Vref in sector I can are given in table 4 as below.

Table 2: Time calculation for V_{ref} in sector I

Region	T_a		T_b		T_c	
1	V_4, V_5	$T_s[2m_a \sin(\frac{\pi}{3} - \theta)]$	V_1, V_2	$T_s[1 - 2m_a \sin(\frac{\pi}{3} + \theta)]$	V_6, V_7	$T_s[2m_a \sin\theta]$
2	V_4, V_5	$T_s[1 - 2m_a \sin\theta]$	V_{17}	$T_s[2m_a \sin(\frac{\pi}{3} + \theta) - 1]$	V_6, V_7	$T_s[1 - 2m_a \sin(\frac{\pi}{3} - \theta)]$
3	V_4, V_5	$T_s[2 - 2m_a \sin(\frac{\pi}{3} + \theta)]$	V_{17}	$T_s[2m_a \sin\theta]$	V_{16}	$T_s[2m_a \sin(\frac{\pi}{3} - \theta) - 1]$
4	V_{18}	$T_s[2m_a \sin\theta - 1]$	V_{17}	$T_s[2m_a \sin(\frac{\pi}{3} - \theta)]$	V_6, V_7	$T_s[2 - 2m_a \sin(\frac{\pi}{3} + \theta)]$

The calculated times remain same for sectors (II to VI) shown in Table 2.

5 RELATIONSHIP BETWEEN V_{REF} LOCATION AND TIME

The relationship can be observed between V_{ref} Location and time shown in fig 3. By assuming the location of V_{ref} at point Q located at the center of region 3. Because the distances for the nearest vectors V_5 and V_7 , V_{17} from Q are the same, the times for these vectors should be identical.

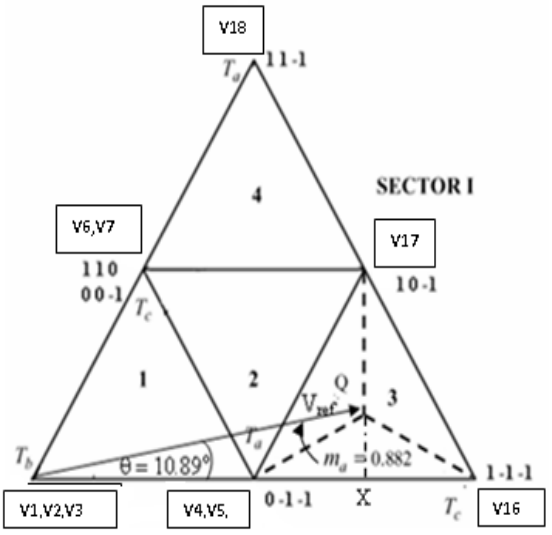

Fig 3: An example to determine the relationship between the location of V ref and times[6].

Three triangles in region 3 are equilibrium triangles. From triangle V_0 ,X, and Q Vref =0.5V_d , and θ = 10.89° . By substituting in equation (6), m_a = 0.8 and $T_a = T_b = T_c = 0.3333T_s$ from the equations in table.4.

6 THE SWITCHING STATES BY USING SWITCHING SEQUENCE

By considering the switching transition and using sequences direction, shown in Fig.4. and Fig.5, the direction of the switching sequences for all regions in six sectors can be derived and the switching orders are known, which are obtained for each region located in sectors I to VI, if all switching states in each region are used.

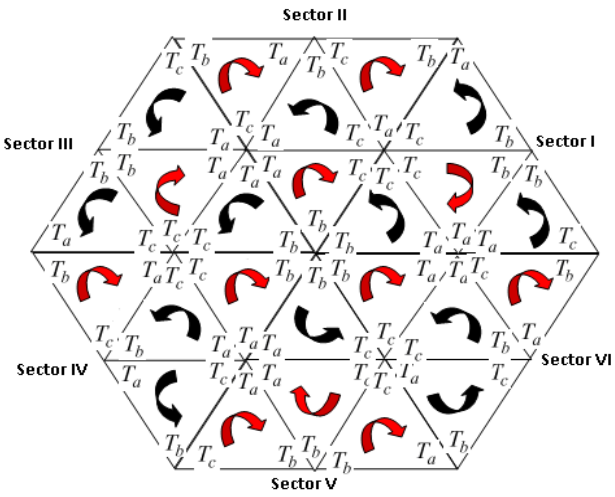

Fig 4: Switching sequence for three-level SVPWM inverter[4]

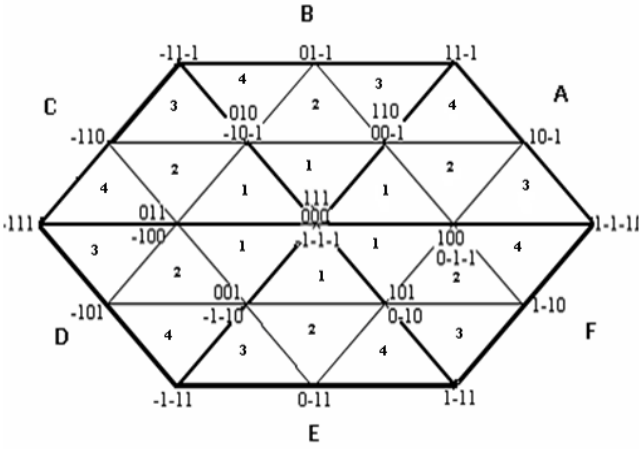

Fig 5: Sectors and their regions for three-level inverter [10]

7 DESIGN AND CONTROL OF AN L & LCL-FILTER FOR THREE-LEVEL INVERTER

The reduction of the current harmonics around switching frequency and multiplication of switching frequency is done to achieve compliance with grid codes as IEEE 519-1992. High inductance values can achieve this goal; however, inductor is bulky, expensive and will limit the converter dynamics as well as the total operating range. The voltage drop across the inductance is controlled by the fundamental component of the PWM converter voltage with its maximal amplitude limited by the DC-link voltage. Consequently, a high current through the inductance requires either a high dc-link voltage or a low inductance. The maximal inductance can be determinate to

$$L < \sqrt{\frac{Vdc^2 - UGm^2}{\omega I_m}} \qquad (10)$$

Where

u_{dc} – dc- link voltage,

U_{Gm} – amplitude of grid voltage,

I_m – amplitude of current,

ω - angular frequency of the grid.

The application of a LCL low pass filter (Fig.6) with a relatively small filter size and a good decoupling of the filter performance from grid impedance variations provides a good performance. It can be seen that the ac filter can be smaller / less heavy for a three-level topology for any desired current ripple value or harmonic spectrum. Due to the quadratic dependency of ripple current and losses the application of a three-level converter will result in substantially smaller losses in any given inductance.

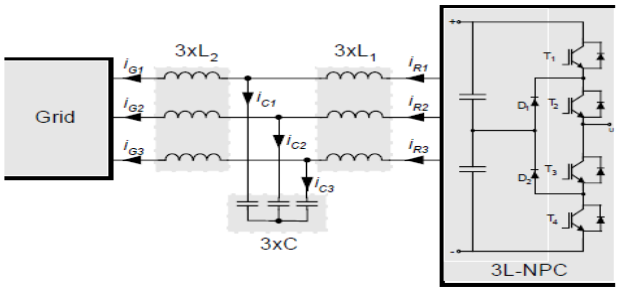

Fig 6: Diagram of a three-phase LCL-filter connected between grid and 3L-NPC PWM rectifier.

This topology consists on just an inductive filter L connected in series with the converter. Although being the topology with the fewer number of components the system dynamics is poor due to the voltage drop across the inductor causing long time responses.

Filter parameters:

Grid side inductance =100 [mH]
Converter side inductance =100[mH]
Capacitor (star connection) =5 [μF]

Table 3: modulation index versus THD (%) for LCL filter

Amplitude	Modulation	THD(%) of Line to line voltage
150	0.3712	7.0
175	0.4330	11.0
200	0.4949	10.5
225	0.5567	7.2
250	0.6186	5.2
275	0.6804	4.9
300	0.7423	4.5
325	0.8042	3.6
350	0.866	3.5
375	0.9279	3.5
400	0.9897	3.6

Table 4: Modulation index versus THD (%) for L filter

Amplitude	Modulation	THD(%) of Line to line voltage
150	0.3712	2.9
175	0.4330	4.5
200	0.4949	4.8
225	0.5567	3.0
250	0.6186	1.7
275	0.6804	2.1
300	0.7423	1.9
325	0.8042	1.8
350	0.866	2.3
375	0.9279	1.9
400	0.9897	2.2

Table 3 & 4 gives the variation of modulation index versus total harmonic distortion [THD] for LCL and L filter.

Figure 7 and figure 8 shows the variation of Total Harmonic Distortion (%) versus modulation of LCL & L Filters.

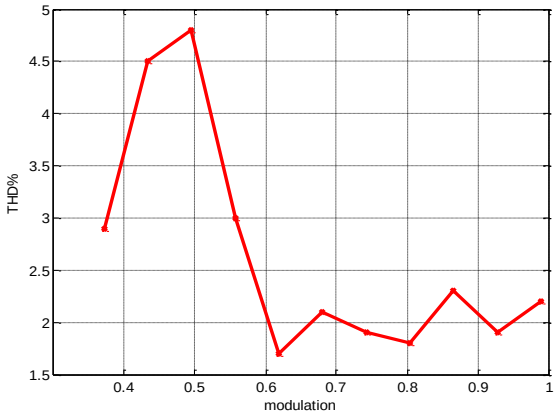

Fig 7: THD% v/s modulation of L filter

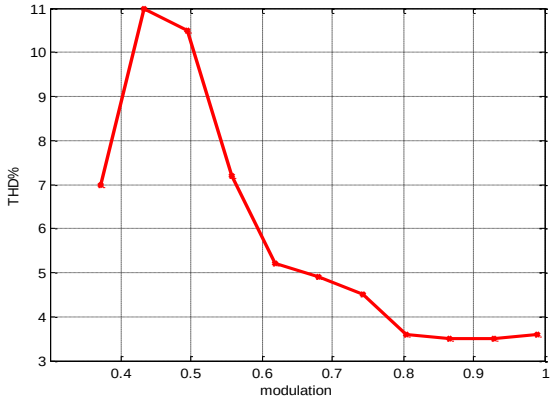

Fig 8: THD% v/s modulation of LCL filter

The output line to line voltage waveform for three phases three level inverter in figure 9.

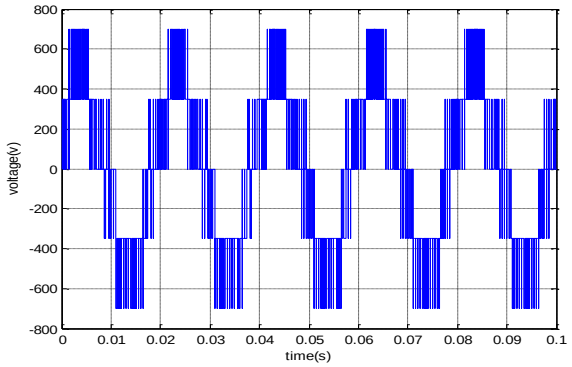

Fig 9: The output line to line voltage waveform for three phase three level inverter

Figure 10 and figure 11 shows the grid side Phase voltage and current of LCL filter respectively. Figure 12 and figure 13 grid side Phase voltage and current of L filter respectively.

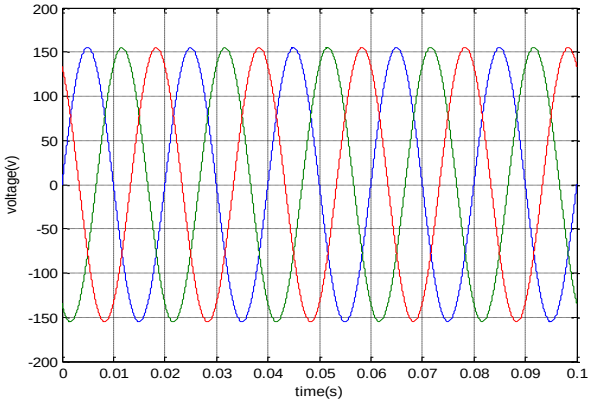

Fig 10: Grid side Phase voltage of LCL filter

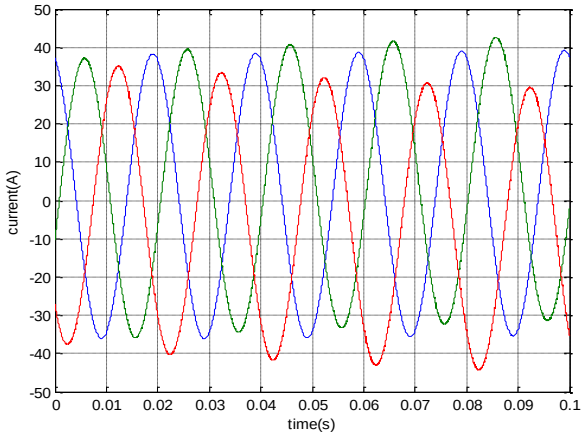

Fig 11: Grid side Phase current of LCL filter

8 SIMULATION RESULTS

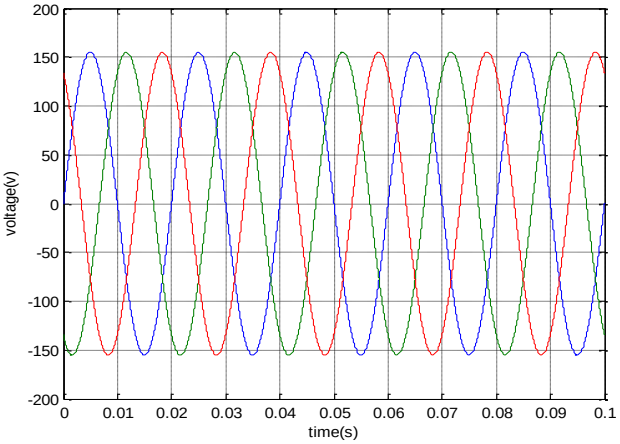

Fig 12: Grid side Phase voltage of L filter

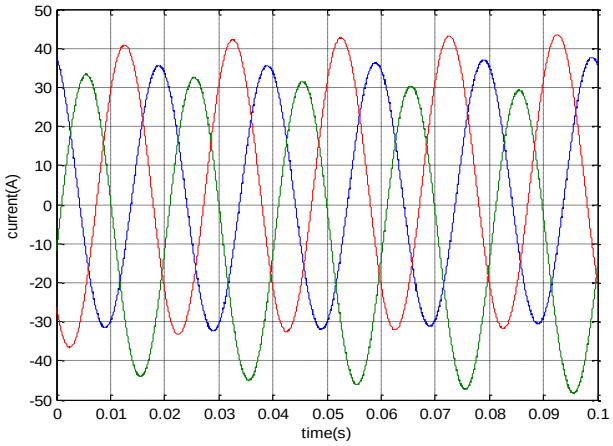

Fig 13: Grid side Phase current of L filter

9 CONCLUSION

An implementation done concerning the application of the SVPWM control strategy on the three-level voltage inverter for L & LCL filters was presented using MATLAB/SIMULINK. Designing of L and LCL filters is done to smooth the inverter output which is connected to grid.
This aimed on the one hand to prove the effectiveness of the SVPWM in the contribution in the switching power losses reduction and to show the advantage of multilevel inverters that carry out voltages with less harmonic content's injection than the comparable two-level inverters on the other hand and design of filters to give sinusoidal output to grid. The obtained simulation results were satisfactory. As prospects, future experimental works will validate the simulation results.

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